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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/657,797	09/08/2003	William C. Moyer	SC13071TH	1577
23125	7590	07/24/2006	EXAMINER	
FREESCALE SEMICONDUCTOR, INC. LAW DEPARTMENT 7700 WEST PARMER LANE MD:TX32/PL02 AUSTIN, TX 78729			PAN, DANIEL H	
		ART UNIT	PAPER NUMBER	
		2183		

DATE MAILED: 07/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/657,797	MOYER ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 11 May 2002.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-43 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-7,10,12,13,15-22,25,27,28 and 30-43 is/are rejected.
- 7) Claim(s) 8,9,11,14,23,24,26,29 is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 02/09/06.
- 4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) Notice of Informal Patent Application (PTO-152)
- 6) Other: _____.

1. Claims 1-43 remain for examination. No change has been made to claims.
2. Claim 1 provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of copending Application No.10/657,331 Although the conflicting claims are not identical, they are not patentably distinct from each other. The reasons already given in the last Office action, therefore, it will not be repeated herein. The response to applicant's remark will follow in the response to a) in this action.
4. Claim 1 provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of copending Application No. 10/657,510 Although the conflicting claims are not identical, they are not patentably distinct from each other. The reasons already given in the last Office action, therefore, it will not be repeated herein. The response to applicant's remark will follow in the response to a) in this action.
5. Claims 1, 2,6,7,10,12,16,17, 19,20,21,25,27 are rejected under 35 U.S.C. 102(b) as being anticipated by Inagami et al. (4,760,545).
6. Claims 3-5 , 18, 34,37, 40,43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inagami (4,760,545) in view of Omoda et al. (4,825,361) .
7. Claims 13, 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inagami (4,760,545) in view of Betker et al. (6,052,766).
8. Claim 15, 30, 31 , 32 ,33,35,36,38,39,41 ,42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inagami (4,760,545) in view of Blomgren et al. (6,898,691).

9. The rejections are maintained and incorporated by reference the last office action on 02/16/06.
10. The response filed on 05/11/06 has been fully considered but is not persuasive.
11. In the remarks, applicant argued that :
12. a) the second offset is not a starting location of the register , but is an offset between the first portion and second portion of the data element in the memory. The second offset is between the portions of data elements in the memory not in the register;
13. b) D1 provides an offset for a starting element from the start of a vector register, not but does not provide an offset between two portions of data element in the memory;
14. c) the block4v instruction may be used to implement the bit reverse Fast Fourier Transform, but Blomgren did not teach the radix specified within the instruction itself;
15. d) claims recite a single instruction (i.e. one instruction) to implement the reversed transfer;
16. e) no suggestion to include radix specifier in an instruction or to provide single instruction which can implement bit-reverse transfers between memory and registers .
- 17.
18. As to a) above, a starting location of the register is an offset between the first portion before the starting location and second portion (after the starting location) of the data element in the memory. Therefore, the second offset is between the portions of the data elements. As to the elements on the memory , not in the register. Examiner

holds that registers are components of a memory in the hardware level. Therefore, there is no distinction between memory and register unless applicant can show his memory is not using registers.

19. As to b) , D1 provides an offset for a starting element from the start of a vector register, and this offset is between two portions of data element (the vector portion before starting location and the portion after the starting location). Therefore, D1 was an offset between the two portions. As to the memory, see the discussions to a) above.

20. As to c), Blomgren's block4v instruction used to implement the bit reverse Fast Fourier Transform. The bit reversal was already a radix bit (see col.11, lines 34-42). Therefore, Blomgren did teach the radix specifier within the single instruction itself. In addition, applicant already admitted that the radix parameter may be used to load a series of data into a register or set of registers according to an FFT addressing algorithm, as known in the art (see Paragraph 00125 in the published specification).

21. As to d), applicant's claims (e.g. claim 15) recite one or more instructions, not single instruction. applicant is reminded that unclaimed features cannot be used to overcome the prior art (e.g. see CCPA In re Lundenberg & Zuschlag, 113, USPQ 530, 534 (1957)).

22. As to e) , see response to c) and d) above. Transfer between memory and register had been known , such as the load.

23. Claims 8,9 ,23 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the combined features of specifying a total number of data elements to be transferred between the memory and both the first and second registers.

24. Claims 11 ,24 , 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the combined features of filing at least a portion of any remaining bit locations either predetermined value if the total number of data elements transferred does not completely fill the second register.

25. Claims 14 , 29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the combined features of the specifier the second offset used more than once if the first number of data elements to be transferred is larger than twice the first portion of the data elements to be transferred.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

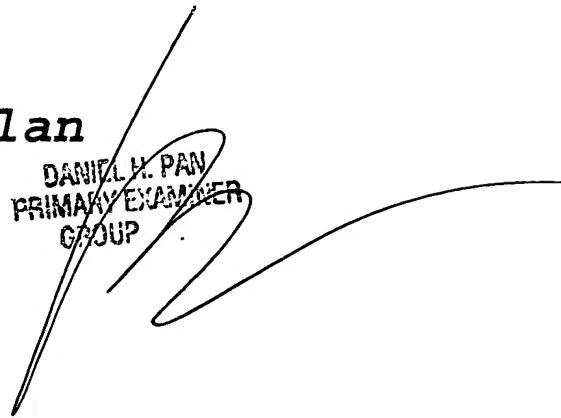
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712; or the new number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21 Century Strategic Plan

DANIEL H. PAN
PRIMARY EXAMINER
GROUP

A handwritten signature in black ink, appearing to read "DANIEL H. PAN", is written over a large, stylized, sweeping "B" that spans across the page.